FIG. 1

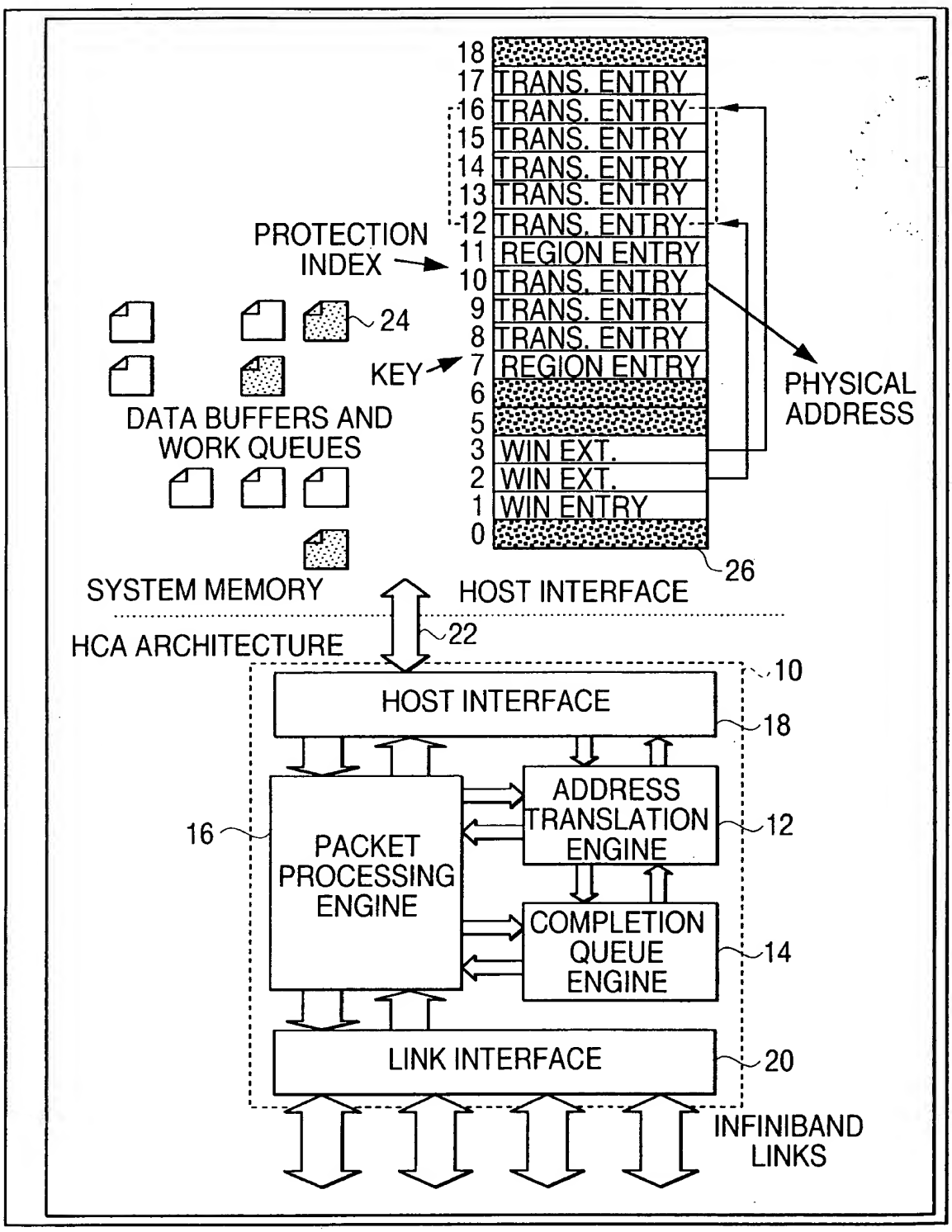

18
17 TRANS. ENTRY
16 TRANS. ENTRY
15 TRANS. ENTRY
14 TRANS. ENTRY
13 TRANS. ENTRY
12 TRANS. ENTRY
11 REGION ENTRY
10 TRANS. ENTRY
9 TRANS. ENTRY
8 TRANS. ENTRY
7 REGION ENTRY
6
5
3 WIN EXT.
2 WIN EXT.
1 WIN ENTRY
0
PROTECTION INDEX
KEY
24
DATA BUFFERS AND WORK QUEUES
PHYSICAL ADDRESS
26
SYSTEM MEMORY
HOST INTERFACE
22
HCA ARCHITECTURE
10
HOST INTERFACE
18
16
PACKET PROCESSING ENGINE
ADDRESS TRANSLATION ENGINE
12
COMPLETION QUEUE ENGINE
14
LINK INTERFACE
20
INFINIBAND LINKS

FIG. 2

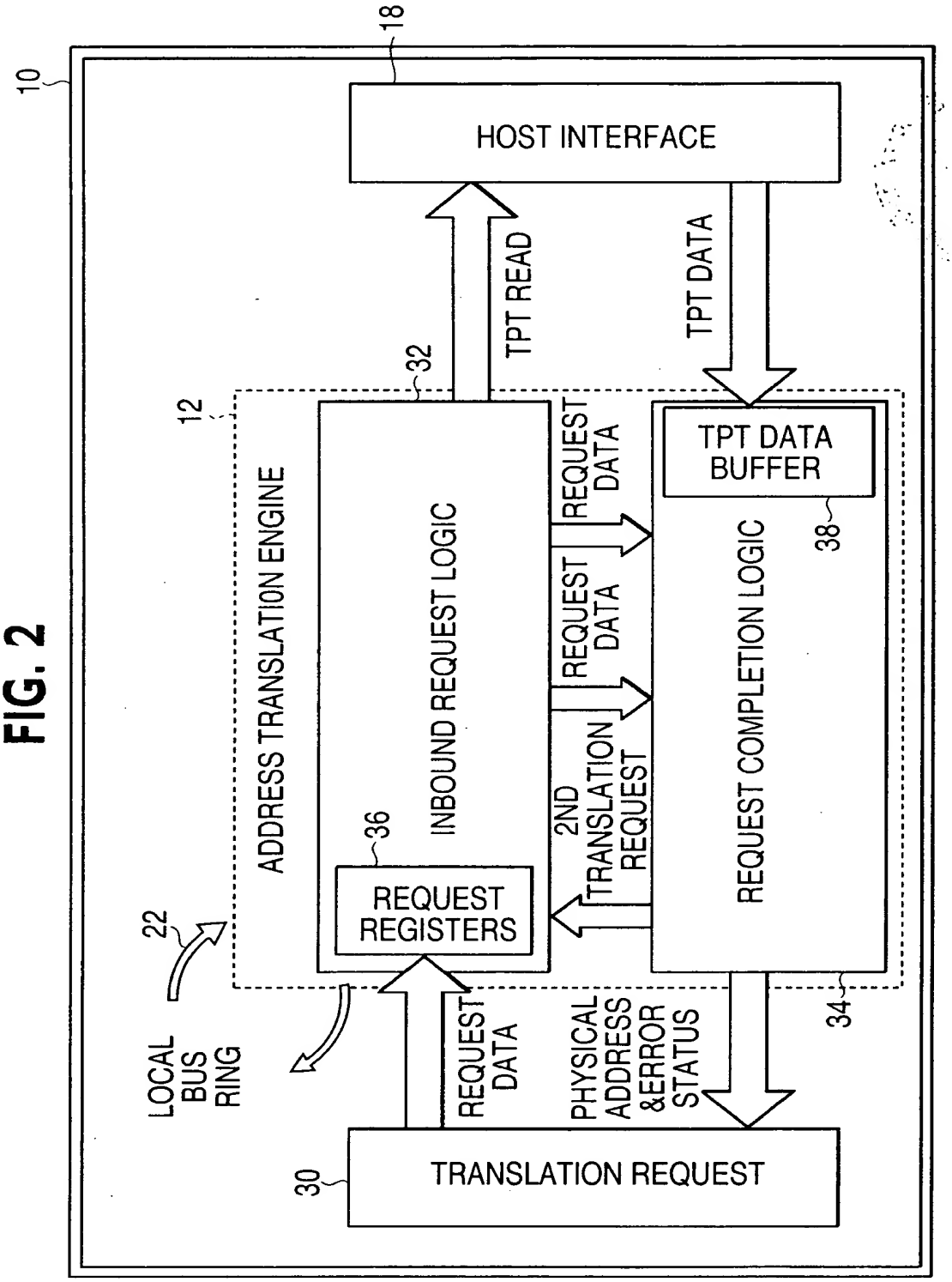

10
18
HOST INTERFACE
TPT READ
TPT DATA
32
12
ADDRESS TRANSLATION ENGINE
INBOUND REQUEST LOGIC
REQUEST DATA
TPT DATA BUFFER
38
REQUEST DATA
REQUEST COMPLETION LOGIC
2ND TRANSLATION REQUEST
36
REQUEST REGISTERS
22
LOCAL BUS RING
REQUEST DATA
PHYSICAL ADDRESS &ERROR STATUS
34
30
TRANSLATION REQUEST

FIG. 3

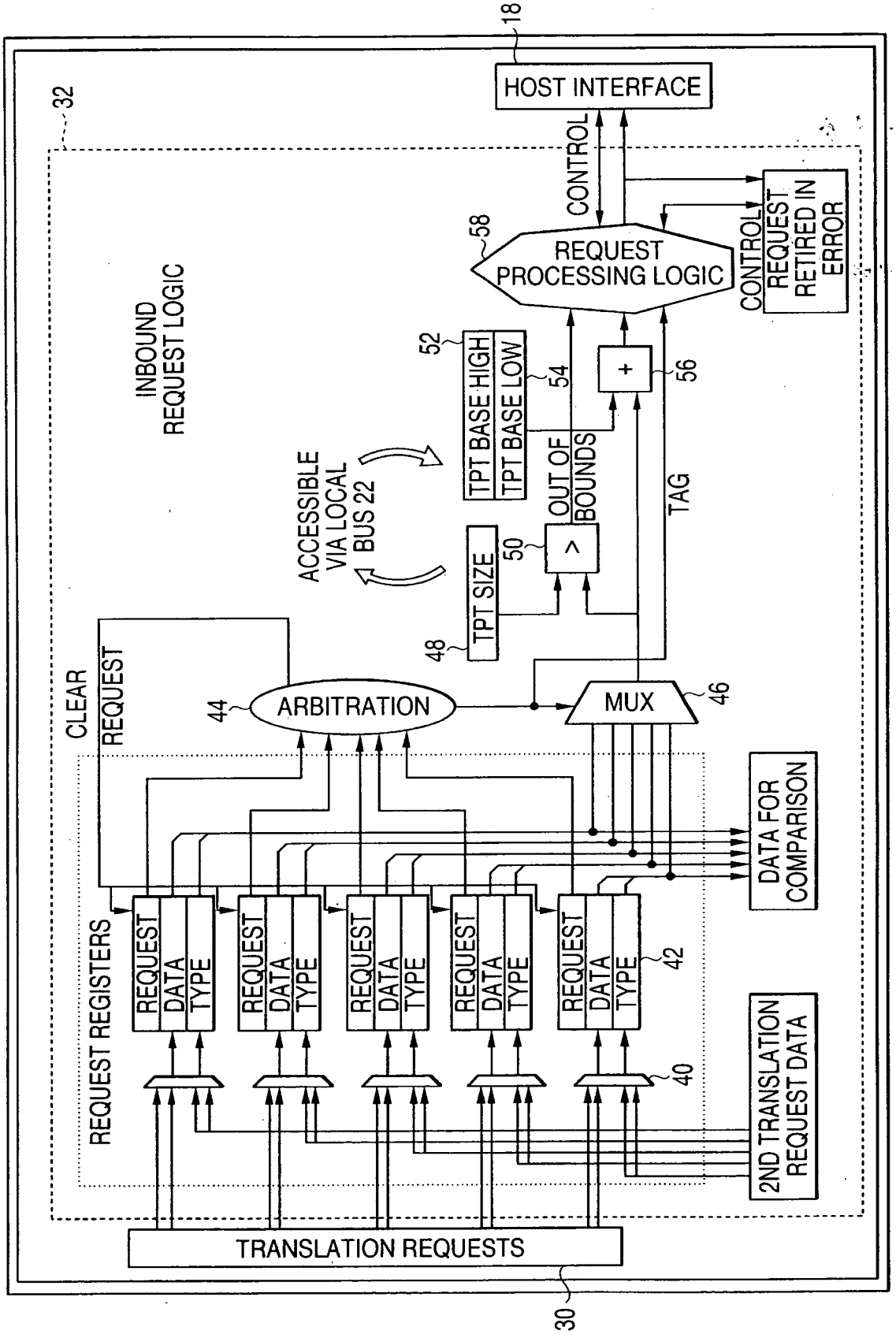

18
HOST INTERFACE
32
CONTROL
58
REQUEST PROCESSING LOGIC
CONTROL
REQUEST RETIRED IN ERROR
INBOUND REQUEST LOGIC
52
TPT BASE HIGH
TPT BASE LOW
54
+
56
ACCESSIBLE VIA LOCAL BUS 22
OUT OF BOUNDS
TAG
50
>
48
TPT SIZE
CLEAR REQUEST
44
ARBITRATION
MUX
46
DATA FOR COMPARISON
REQUEST REGISTERS
REQUEST
DATA
TYPE
42
40
2ND TRANSLATION REQUEST DATA
TRANSLATION REQUESTS
30

FIG. 4

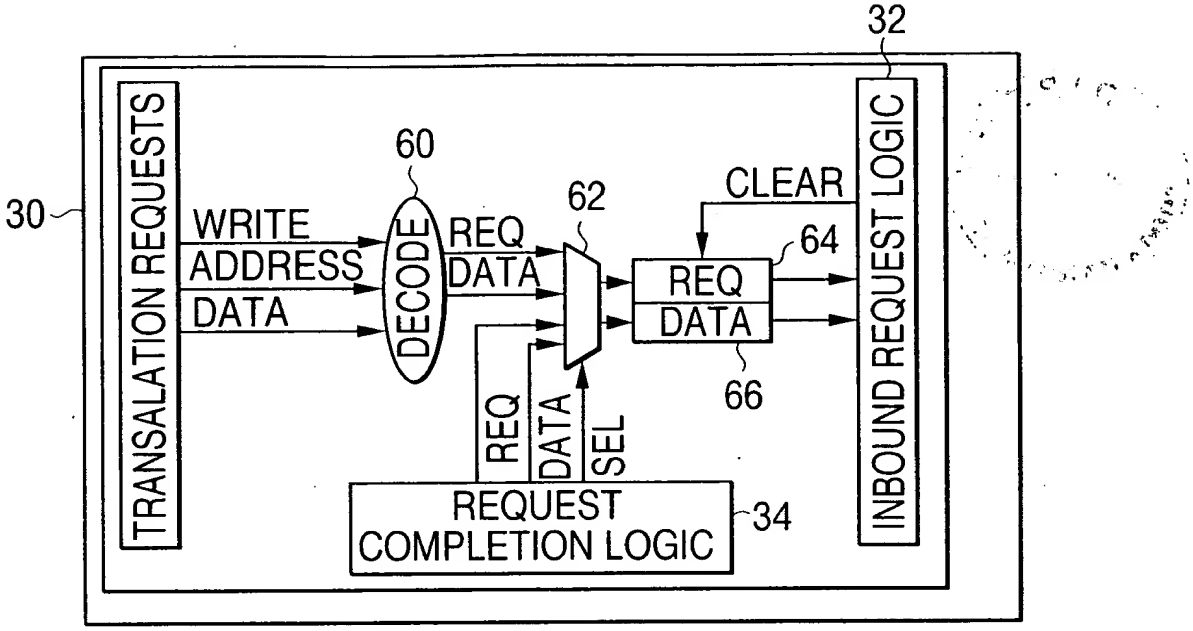

32
30
TRANSALATION REQUESTS
60
WRITE
ADDRESS
DATA
DECODE
REQ
DATA
62
CLEAR
64
REQ
DATA
66
INBOUND REQUEST LOGIC
REQ
DATA
SEL
REQUEST
COMPLETION LOGIC
34

FIG. 5

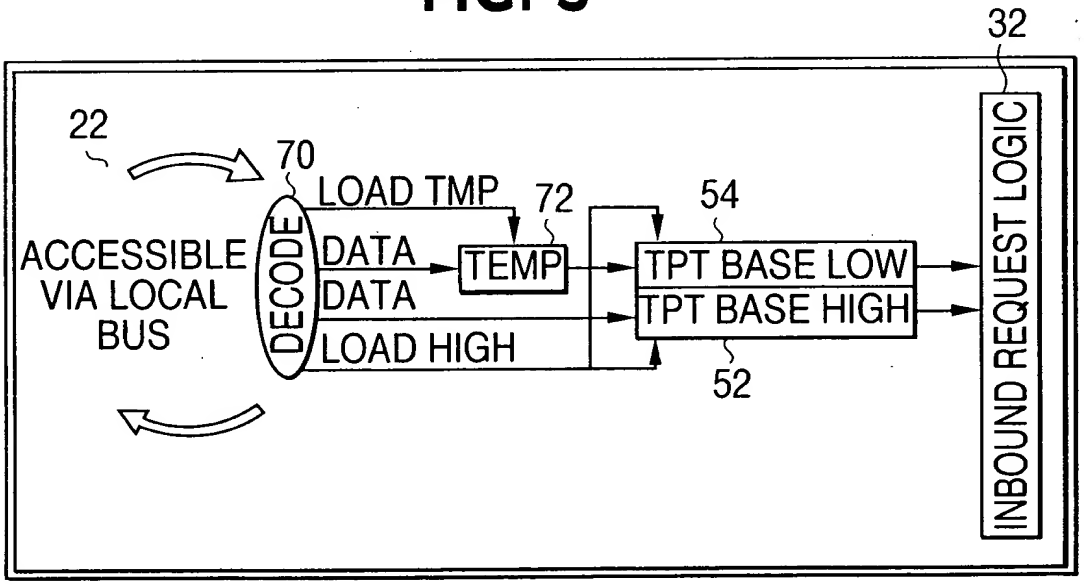

32
22
70
LOAD TMP
72
54
ACCESSIBLE
VIA LOCAL
BUS
DECODE
DATA
DATA
LOAD HIGH
TEMP
TPT BASE LOW
TPT BASE HIGH
52
INBOUND REQUEST LOGIC

FIG. 6

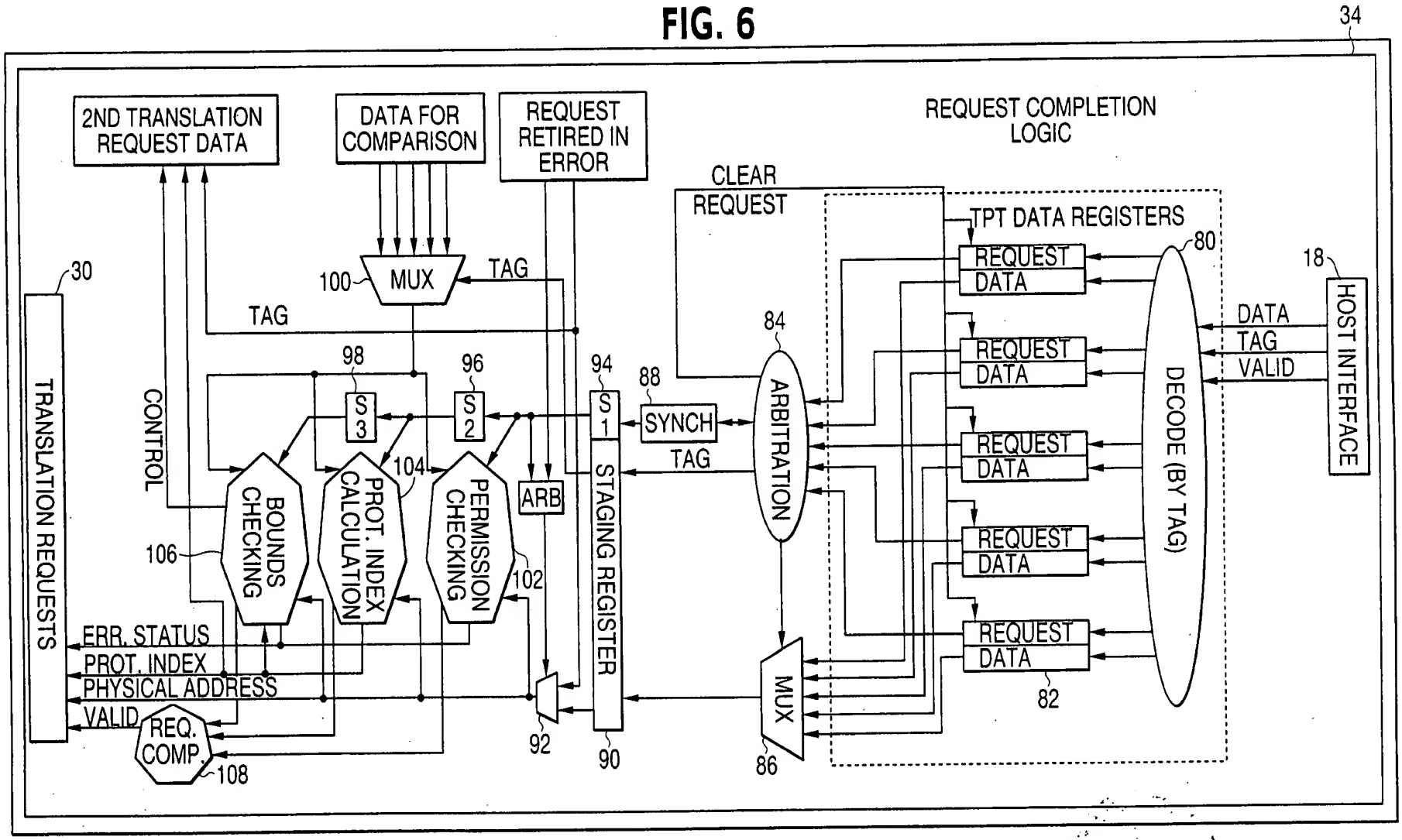

34
2ND TRANSLATION REQUEST DATA
DATA FOR COMPARISON
REQUEST RETIRED IN ERROR
REQUEST COMPLETION LOGIC
CLEAR REQUEST
TPT DATA REGISTERS
30
TRANSLATION REQUESTS
100
MUX
TAG
TAG
98
96
94
88
84
80
18
HOST INTERFACE
DATA
TAG
VALID
CONTROL
S 3
S 2
S 1
SYNCH
TAG
ARBITRATION
DECODE (BY TAG)
REQUEST
DATA
104
BOUNDS CHECKING
PROT. INDEX CALCULATION
PERMISSION CHECKING
ARB
STAGING REGISTER
106
102
ERR. STATUS
PROT. INDEX
PHYSICAL ADDRESS
VALID
REQ. COMP.
108
92
90
86
82

FIG. 7

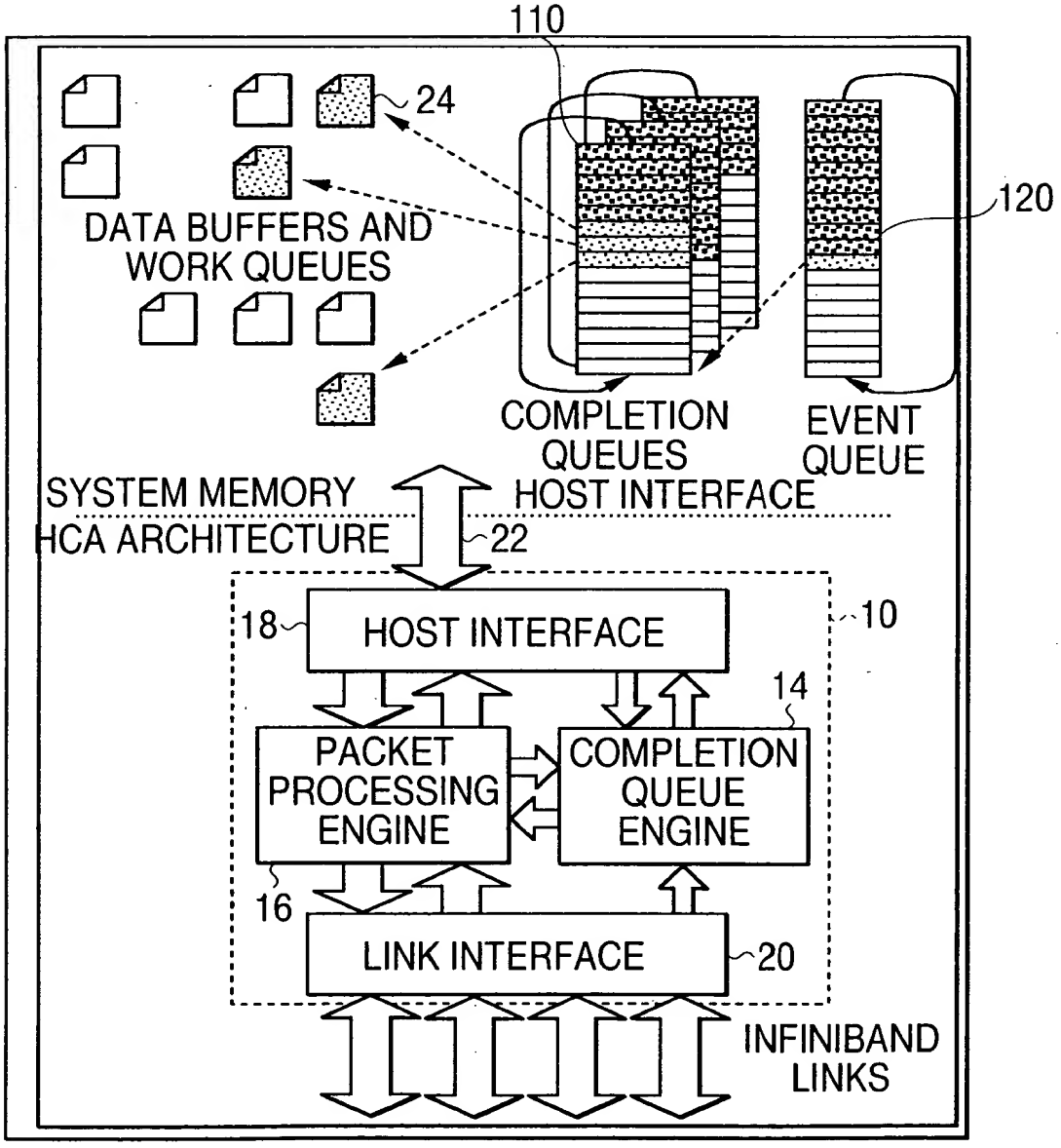

110
24
DATA BUFFERS AND
WORK QUEUES
120
COMPLETION
QUEUES
EVENT
QUEUE
SYSTEM MEMORY
HCA ARCHITECTURE
HOST INTERFACE
22
18
HOST INTERFACE
10
14
PACKET
PROCESSING
ENGINE
COMPLETION
QUEUE
ENGINE
16
LINK INTERFACE
20
INFINIBAND
LINKS

FIG. 8

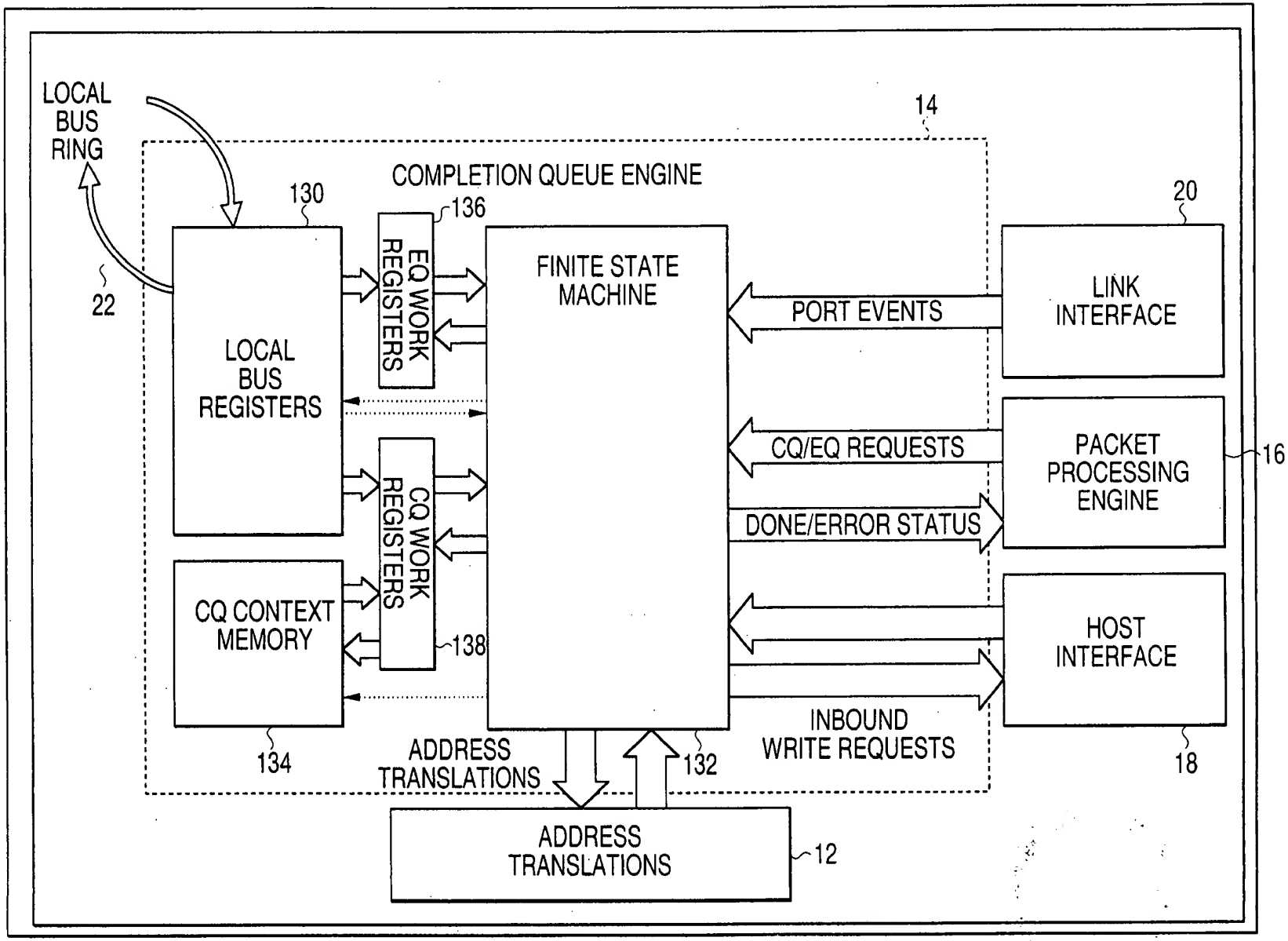

LOCAL BUS RING
22
14
COMPLETION QUEUE ENGINE
130
136
EQ WORK REGISTERS
LOCAL BUS REGISTERS
CQ WORK REGISTERS
138
CQ CONTEXT MEMORY
134
FINITE STATE MACHINE
132
ADDRESS TRANSLATIONS
ADDRESS TRANSLATIONS
12
PORT EVENTS
CQ/EQ REQUESTS
DONE/ERROR STATUS
INBOUND WRITE REQUESTS
20
LINK INTERFACE
PACKET PROCESSING ENGINE
16
HOST INTERFACE
18

FIG. 9

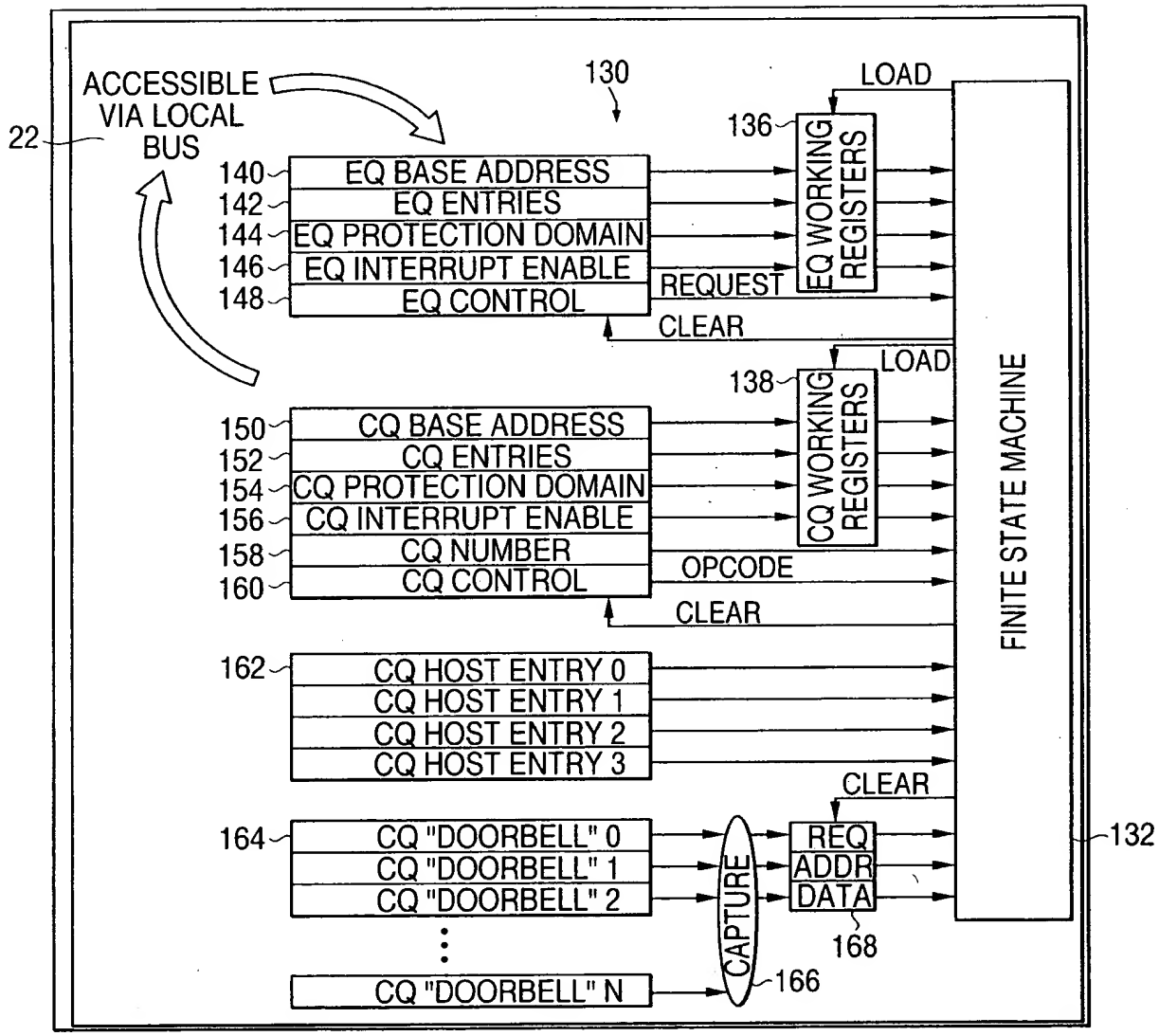

ACCESSIBLE VIA LOCAL BUS
22
130
LOAD
136
EQ WORKING REGISTERS
140 EQ BASE ADDRESS
142 EQ ENTRIES
144 EQ PROTECTION DOMAIN
146 EQ INTERRUPT ENABLE
148 EQ CONTROL
REQUEST
CLEAR
LOAD
138
CQ WORKING REGISTERS
150 CQ BASE ADDRESS
152 CQ ENTRIES
154 CQ PROTECTION DOMAIN
156 CQ INTERRUPT ENABLE
158 CQ NUMBER
160 CQ CONTROL
OPCODE
CLEAR
162
CQ HOST ENTRY 0
CQ HOST ENTRY 1
CQ HOST ENTRY 2
CQ HOST ENTRY 3
CLEAR
164
CQ "DOORBELL" 0
CQ "DOORBELL" 1
CQ "DOORBELL" 2
CQ "DOORBELL" N
CAPTURE
166
REQ
ADDR
DATA
168
FINITE STATE MACHINE
132

FIG. 10

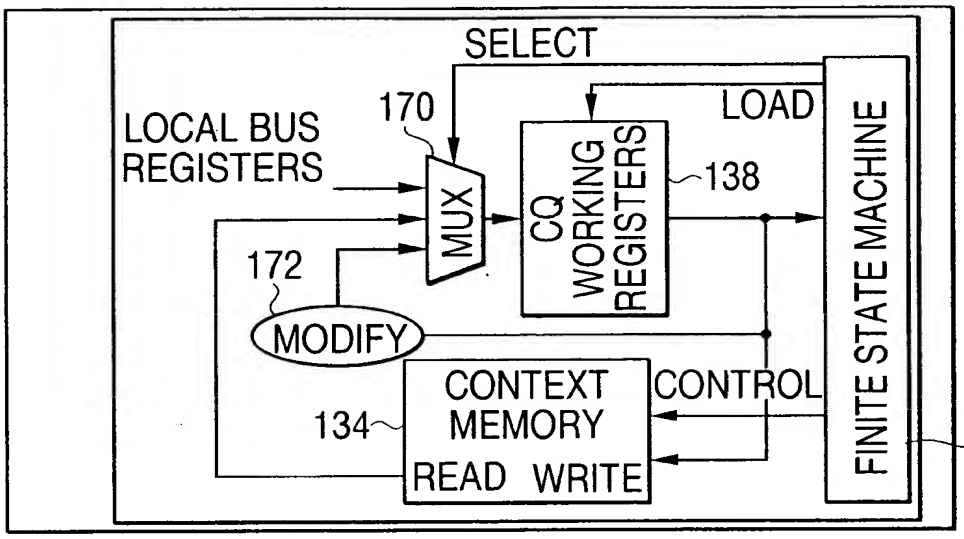


FIG. 11

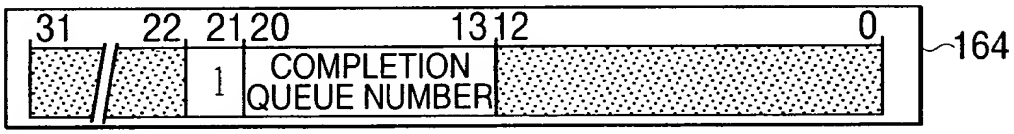


FIG. 12

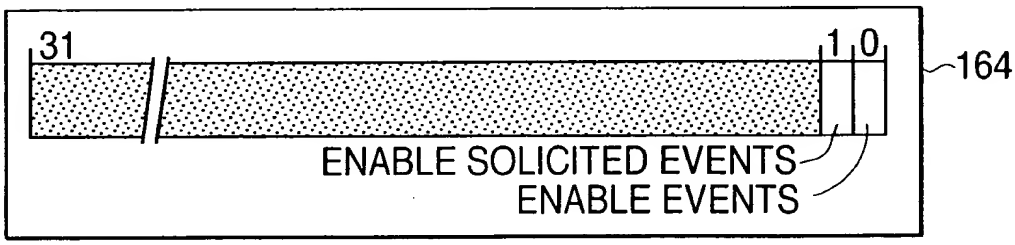
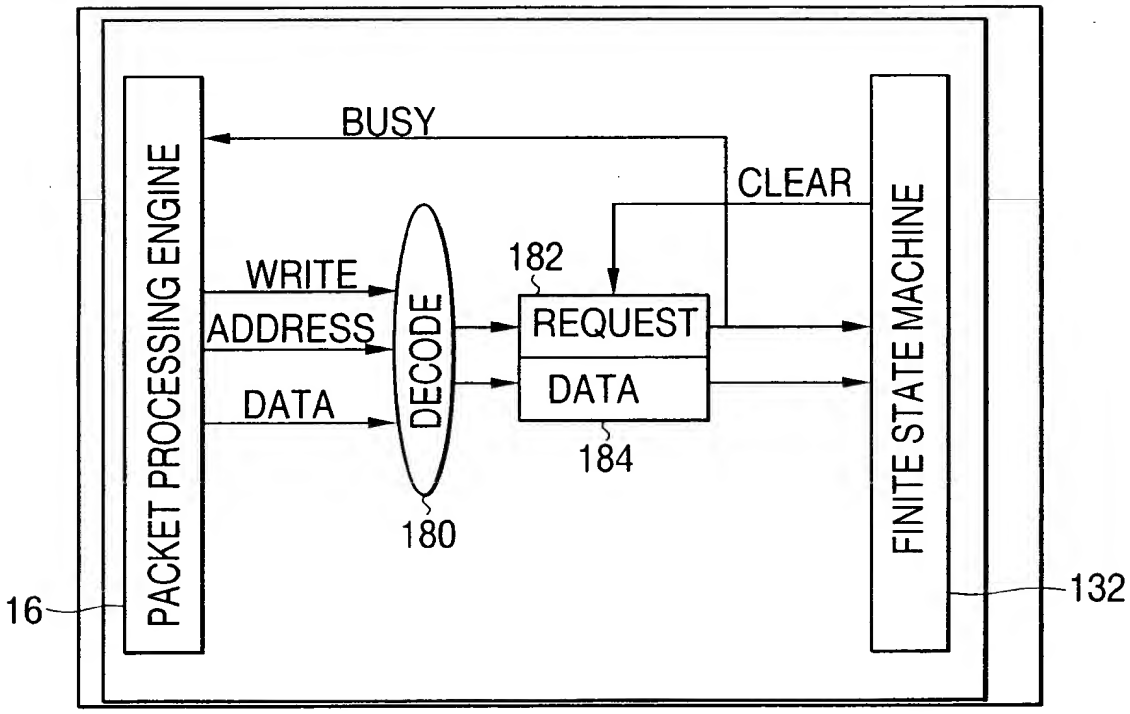


FIG. 13


PACKET PROCESSING ENGINE
BUSY
CLEAR
WRITE
ADDRESS
DATA
DECODE
182
REQUEST
DATA
184
180
FINITE STATE MACHINE
16
132

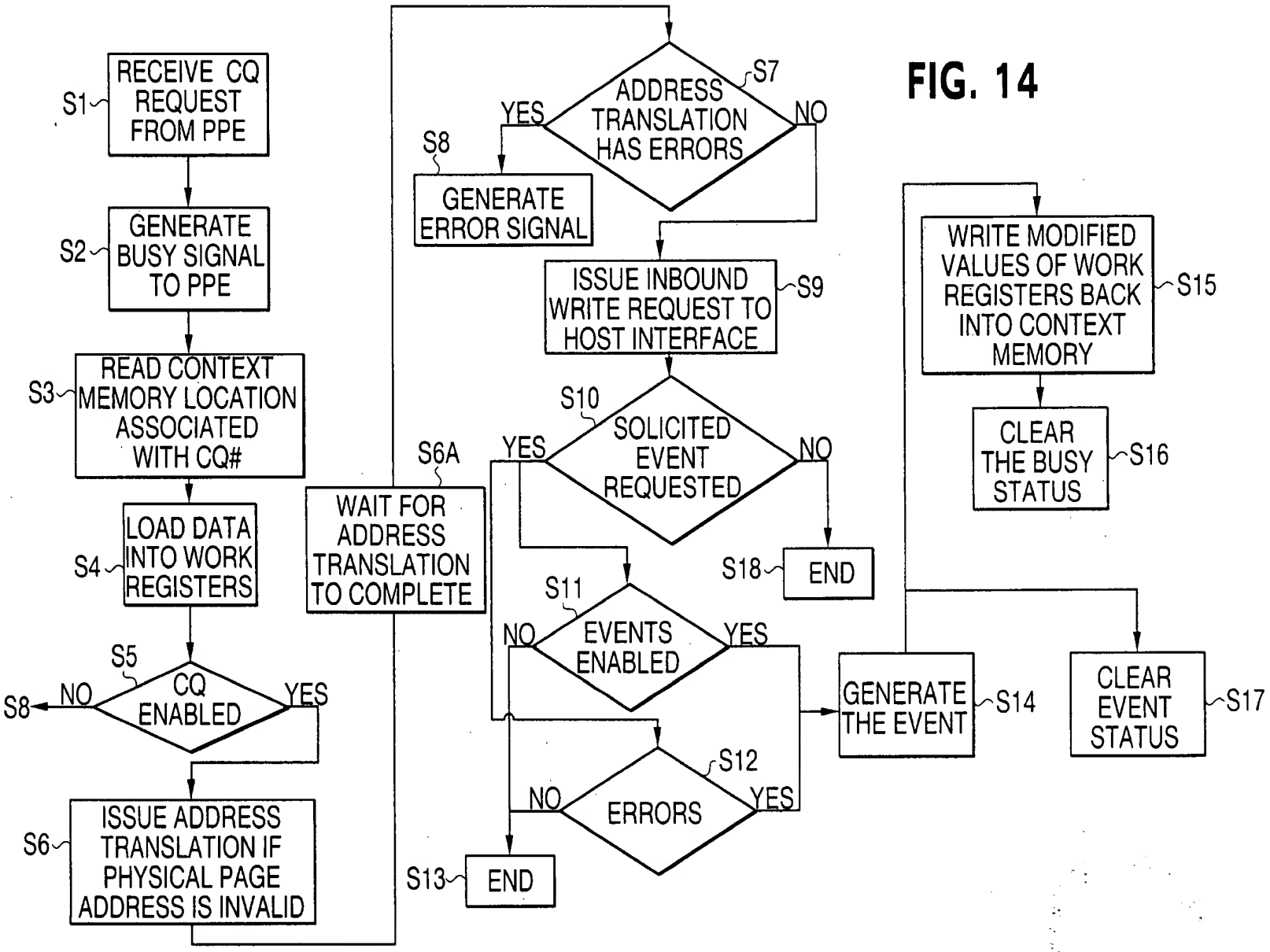

RECEIVE CQ REQUEST FROM PPE
S1
GENERATE BUSY SIGNAL TO PPE
S2
READ CONTEXT MEMORY LOCATION ASSOCIATED WITH CQ#
S3
LOAD DATA INTO WORK REGISTERS
S4
S5
CQ ENABLED
NO
YES
S8
ISSUE ADDRESS TRANSLATION IF PHYSICAL PAGE ADDRESS IS INVALID
S6
WAIT FOR ADDRESS TRANSLATION TO COMPLETE
S6A
S7
ADDRESS TRANSLATION HAS ERRORS
YES
NO
S8
GENERATE ERROR SIGNAL
ISSUE INBOUND WRITE REQUEST TO HOST INTERFACE
S9
S10
SOLICITED EVENT REQUESTED
YES
NO
S18
END
S11
EVENTS ENABLED
NO
YES
S12
ERRORS
NO
YES
S13
END
GENERATE THE EVENT
S14
WRITE MODIFIED VALUES OF WORK REGISTERS BACK INTO CONTEXT MEMORY
S15
CLEAR THE BUSY STATUS
S16
CLEAR EVENT STATUS
S17

FIG. 14

FIG. 15

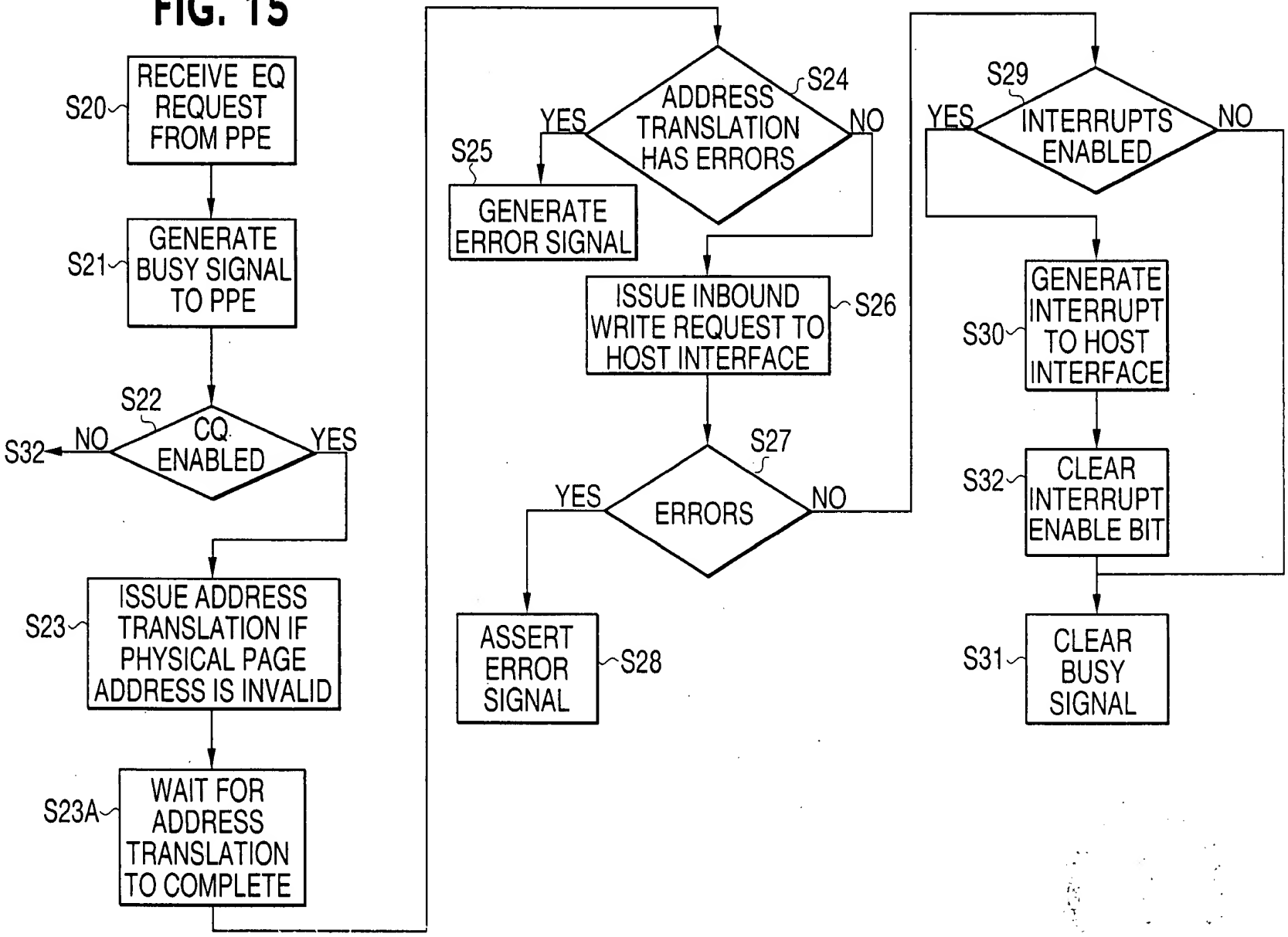

S20
RECEIVE EQ REQUEST FROM PPE
S21
GENERATE BUSY SIGNAL TO PPE
S22
CQ ENABLED
NO
YES
S32
S23
ISSUE ADDRESS TRANSLATION IF PHYSICAL PAGE ADDRESS IS INVALID
S23A
WAIT FOR ADDRESS TRANSLATION TO COMPLETE
S24
ADDRESS TRANSLATION HAS ERRORS
YES
NO
S25
GENERATE ERROR SIGNAL
S26
ISSUE INBOUND WRITE REQUEST TO HOST INTERFACE
S27
ERRORS
YES
NO
S28
ASSERT ERROR SIGNAL
S29
INTERRUPTS ENABLED
YES
NO
S30
GENERATE INTERRUPT TO HOST INTERFACE
S32
CLEAR INTERRUPT ENABLE BIT
S31
CLEAR BUSY SIGNAL

FIG. 16

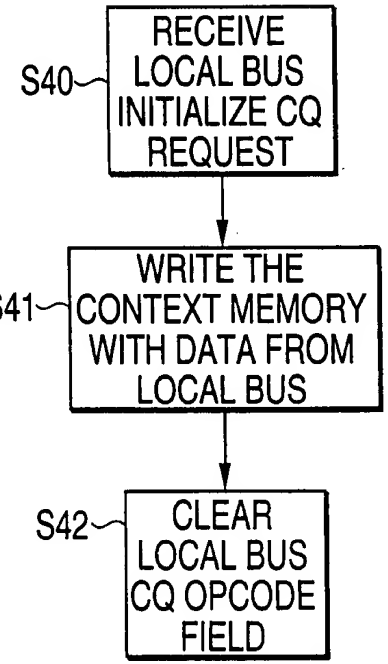


FIG. 17

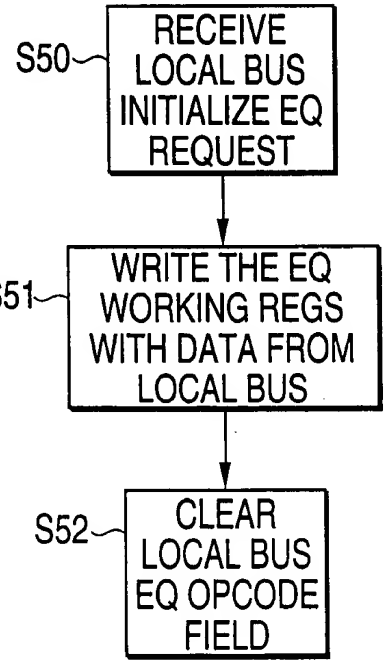


FIG. 18

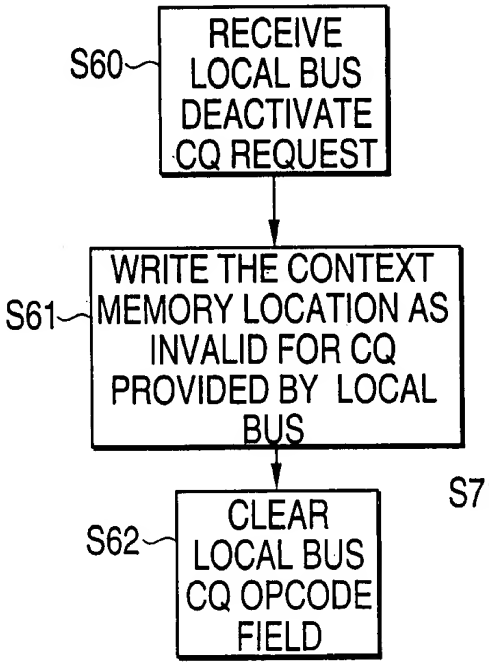


FIG. 19

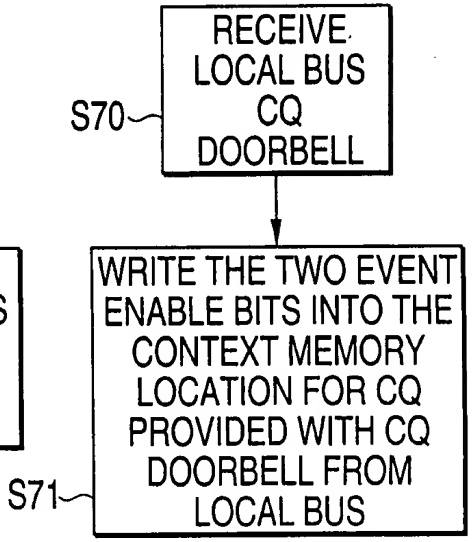
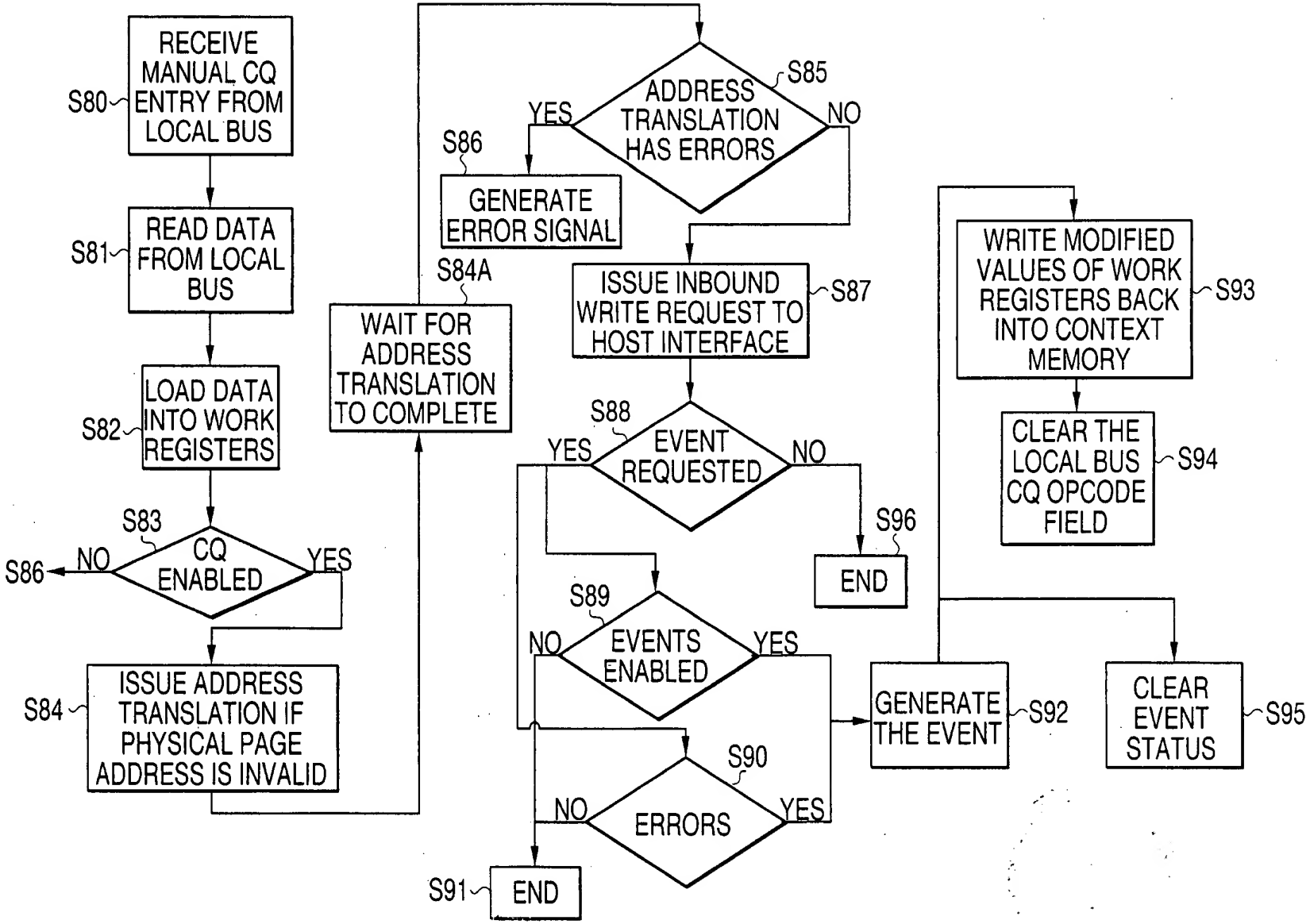


FIG. 20


RECEIVE MANUAL CQ ENTRY FROM LOCAL BUS
S80
READ DATA FROM LOCAL BUS
S81
LOAD DATA INTO WORK REGISTERS
S82
CQ ENABLED
S83
NO
YES
S86
ISSUE ADDRESS TRANSLATION IF PHYSICAL PAGE ADDRESS IS INVALID
S84
WAIT FOR ADDRESS TRANSLATION TO COMPLETE
S84A
ADDRESS TRANSLATION HAS ERRORS
S85
YES
NO
GENERATE ERROR SIGNAL
S86
ISSUE INBOUND WRITE REQUEST TO HOST INTERFACE
S87
EVENT REQUESTED
S88
YES
NO
END
S96
EVENTS ENABLED
S89
NO
YES
ERRORS
S90
NO
YES
END
S91
GENERATE THE EVENT
S92
WRITE MODIFIED VALUES OF WORK REGISTERS BACK INTO CONTEXT MEMORY
S93
CLEAR THE LOCAL BUS CQ OPCODE FIELD
S94
CLEAR EVENT STATUS
S95